SONY

CXD2308Q

10-bit 50MSPS RGB 3-channel D/A Converter

Description

The CXD2308Q is a 10-bit high-speed D/A converter for video band, featuring RGB 3-channel I/O. This is ideal for use in high-definition TVs and high-resolution displays.

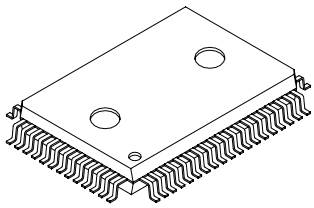
Features

- Resolution 10-bit
- Maximum conversion speed 50MSPS
- RGB 3-channel I/O
- Differential linearity error ±0.5LSB
- Low power consumption 500 mW (Typ.)
- Single +5 V power supply
- Low glitch
- Stand-by function

Structure

Silicon gate CMOS IC

64 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	AV_{DD}, DV_{DD}	7	V
• Input voltage (All pins)	V_{IN}	V_{DD}+0.5 to V_{SS}–0.5	V
• Output current (for each channel)	I_{OUT}	0 to 30	mA
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	V
• Reference input voltage	V_{REF}	1.8 to 2.0	V
• Clock pulse width	T_{PW1},T_{PW0}	9 ns (min.) to 1.1 µs (max.)	
• Operating temperature	Topr	–20 to +75	°C

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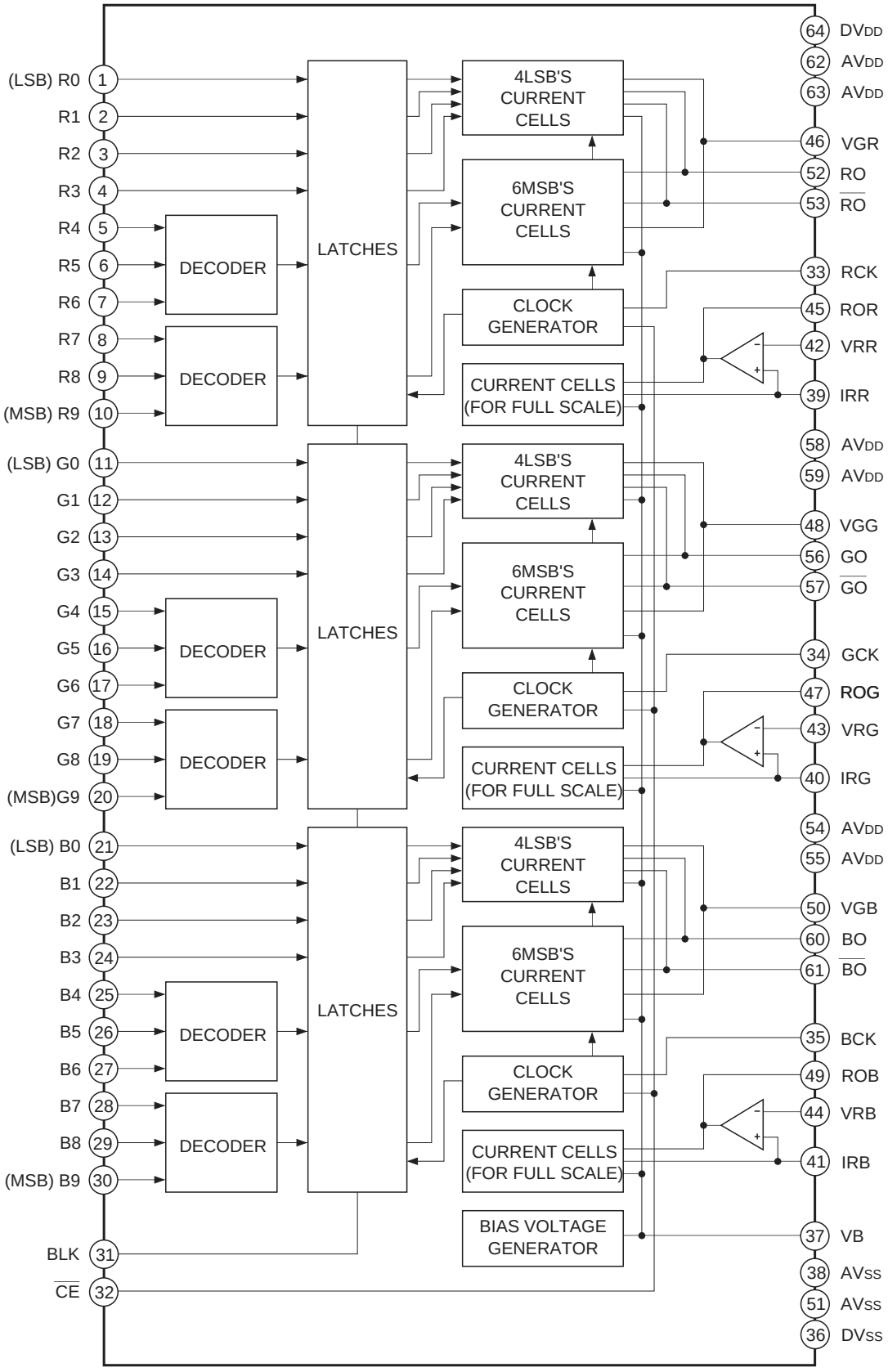
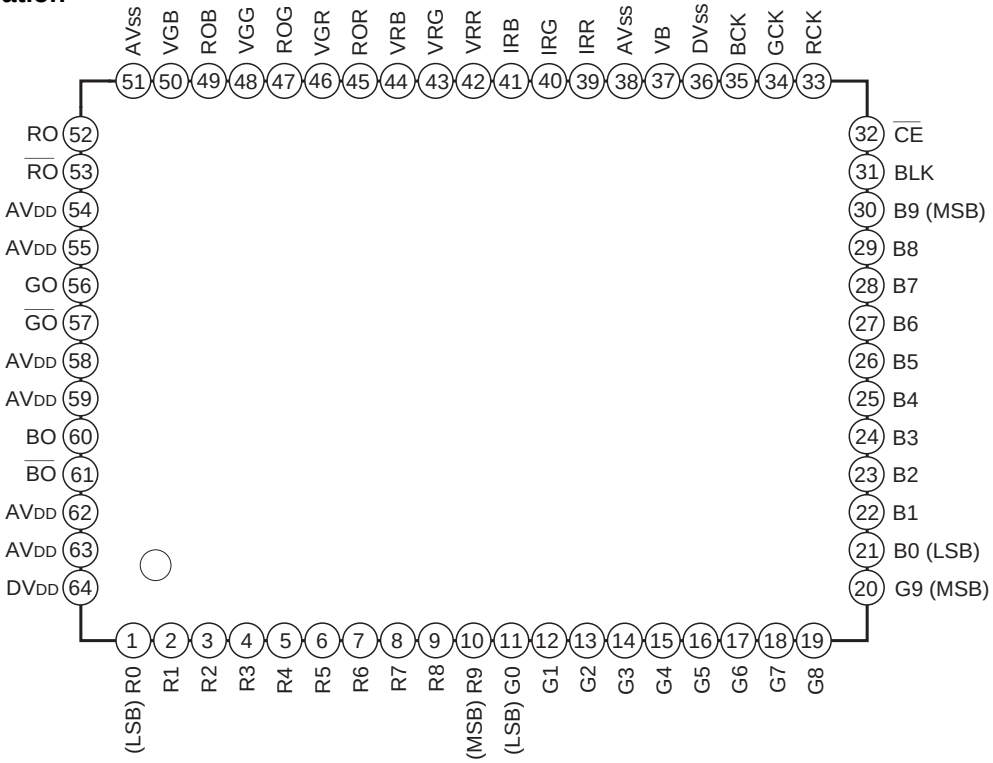
E92929C86-TE

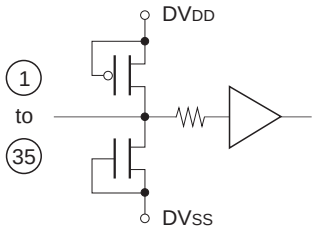
Block Diagram

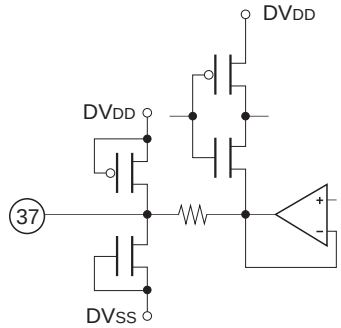
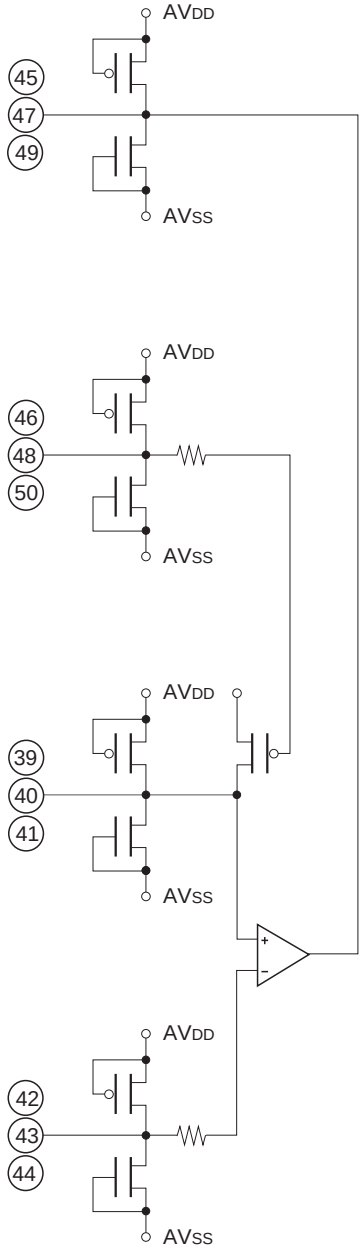


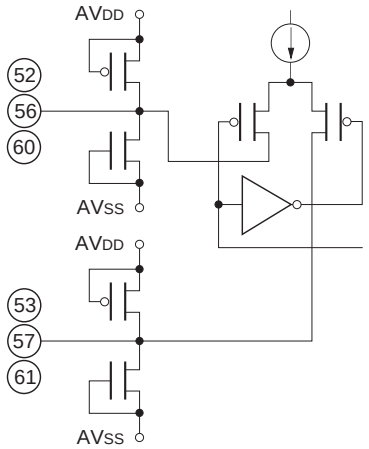
Pin Configuration



Pin Description and Equivalent Circuit

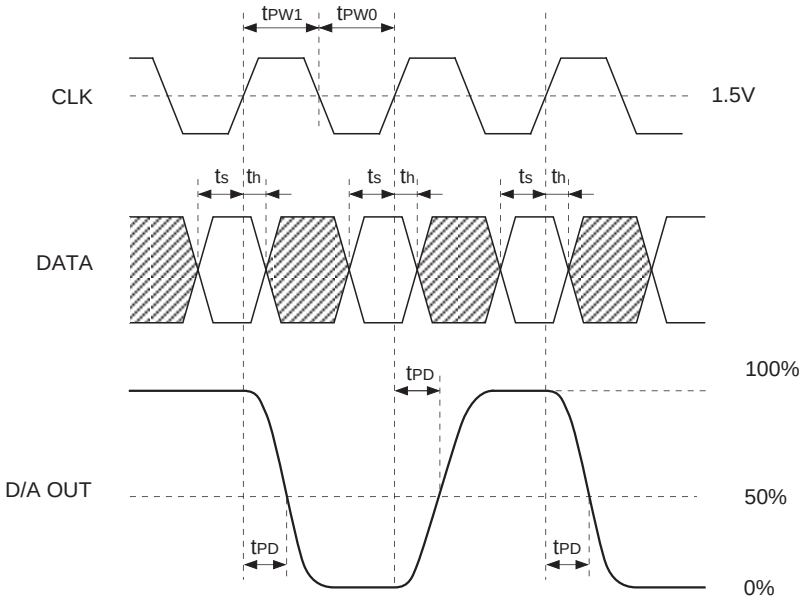
Pin No.	Symbol	I/O	Equivalent circuit	Description
1 to 10	R0 to R9	I		Digital input. R0 (LSB) to R9 (MSB) G0 (LSB) to G9 (MSB) B0 (LSB) to B9 (MSB)
11 to 20	G0 to G9			
21 to 30	B0 to B9			
31	BLK			Blanking input. No signal for High (0 V output). Output generated for Low.
32	$\overline{CE}$			Chip enable input. No signal at for High (0 V output) to minimize power consumption.
33	RCK			Clock inputs.
34	GCK			
35	BCK			
36	DVSS	—		Digital ground.

Pin No.	Symbol	I/O	Equivalent circuit	Description
37	VB			Connect to DVSS with a capacitor of approximately 0.1 µF.
38, 51	AVSS	—		Analog grounds.
45 47 49	ROR ROG ROB	O		Connect to VGR, VGG, and VGB with the control method of output amplitude. See Application Circuit.
46 48 50	VGR VGG VGB	I		Connect a capacitor of approximately 0.1 µF.
39 40 41	IRR IRG IRB	O		Reference current output. Connect to AVSS with a resistance of 1.2 kΩ.
42 43 44	VRR VRG VRB	I		Reference voltage input. Set output full-scale value (2.0 V).

Pin No.	Symbol	I/O	Equivalent circuit	Description
52	RO			Current output. Output can be retrieved by connecting a resistance of 75 Ω to AVSS.
56	GO			
60	BO			
53	$\overline{RO}$			Reverse current output. Normally connected to AVSS.
57	$\overline{GO}$			
61	$\overline{BO}$			
54, 55, 58, 59, 62, 63	AVDD	—		Analog VDD.
64	DVDD			Digital VDD.

Description of Operation

Timing Chart



I/O Correspondence Table (output full-scale voltage: 2.00 V)

Input code	Output voltage
MSB LSB 1 1 1 1 1 1 1 1 1 1	2.0 V
: 1 0 0 0 0 0 0 0 0 0	1.0 V
: 0 0 0 0 0 0 0 0 0 0	0 V

Electrical Characteristics (F_{CLK}=50 MHz, AV_{DD}=DV_{DD}=5 V, R_{OUT}=75 Ω, V_{REF}=2.0 V, Ta=25 °C)

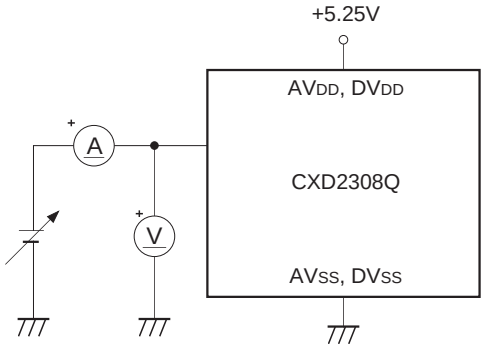
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			10		bit
Conversion speed	F_{CLK}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to +75 °C	0.5		50	MSPS
Integral non-linearity error	E_L	Endpoint	–2.0		2.0	LSB
Differential non-linearity error	E_D		–0.5		0.5	LSB
Precision guaranteed output voltage range	V_{OC}		1.8	1.9	2.0	V
Output full-scale voltage	V_{FS}		1.8	1.9	2.0	V
Output full-scale ratio *1	F_{SR}	For the same gain (See the Application Circuit)	0	1.5	3	%
Output full-scale current	I_{FS}			27	30	mA
Output offset voltage	V_{OS}	When data “0000000000” input			1	mV
Glitch energy	GE			50		pV-s
Crosstalk	CT	When 1 kHz sine wave input		54		dB
Supply current	I_{DD}	$\overline{CE}$= “L”		100	110	mA
	I_{STB}	$\overline{CE}$= “H”			1	
Analog input resistance	R_{IN}	VGR, VGG, VGB, VRR, VRG, VRB	1			MΩ
Input capacitance	C_I				9	pF
Output capacitance	C_O	RO, GO, BO		50		pF
Digital input voltage	V_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to +75 °C	2.15			V
	V_{IL}				0.85	
Digital input current	I_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to +75 °C	–5		5	µA
	I_{IL}					
Setup time	t_s		7			ns
Hold time	t_h		3			ns
Propagation delay time	t_{PD}			10		ns
$\overline{CE}$ enable time *2	t_E	$\overline{CE}$=H→L		1	2	ms
$\overline{CE}$ disable time *2	t_D	$\overline{CE}$=L→H		1	2	ms

*1 Output full-scale ratio = $\left| \frac{\text{Full-scale voltage for each channel}}{\text{Full-scale voltage average value for each channel}} - 1 \right| \times 100\ (\%)$

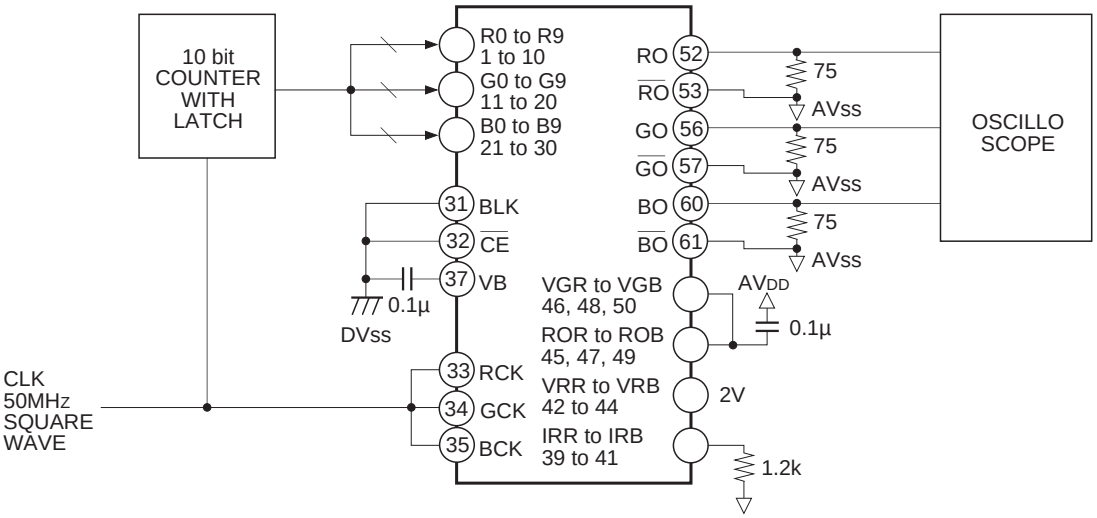
*2 When the external capacitors for the VGR, VGG and VGB pins are 0.1 µF.

Electrical Characteristics Test Circuit

Analog Input Resistance
Digital Input Current } **Test Circuit**

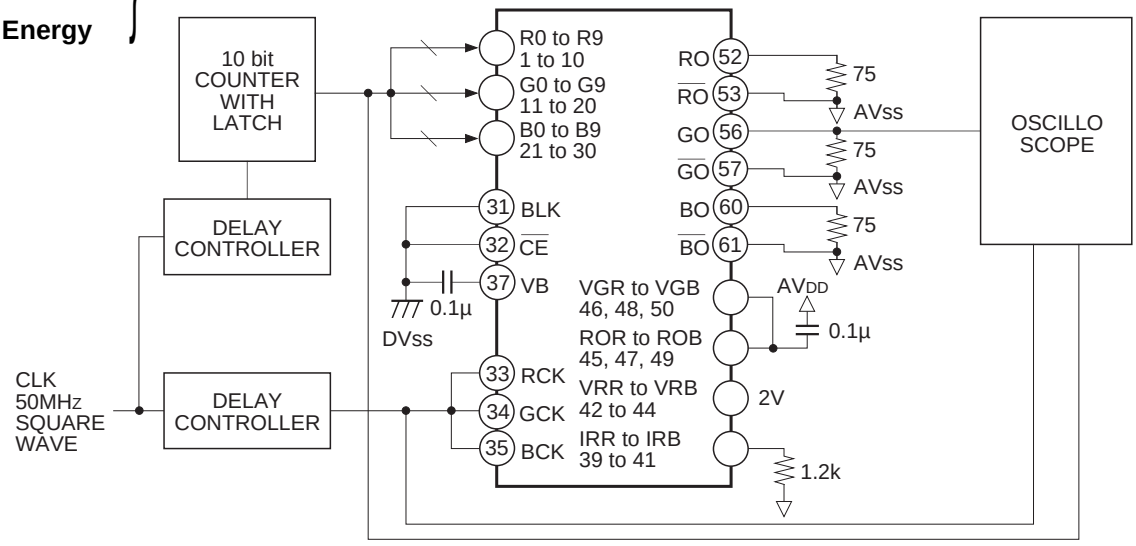


Maximum Conversion Speed Test Circuit

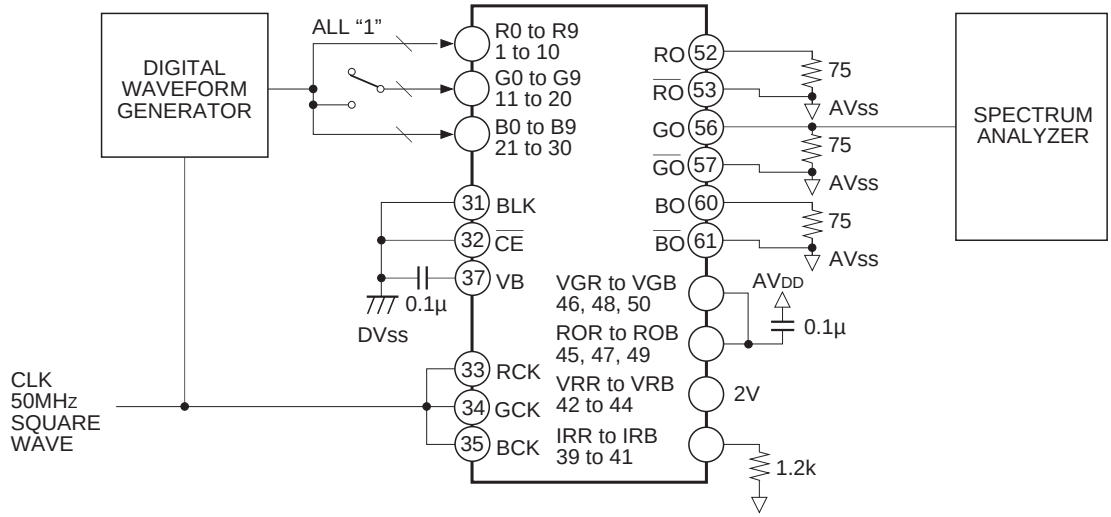


Setup Time
Hold Time
Glitch Energy

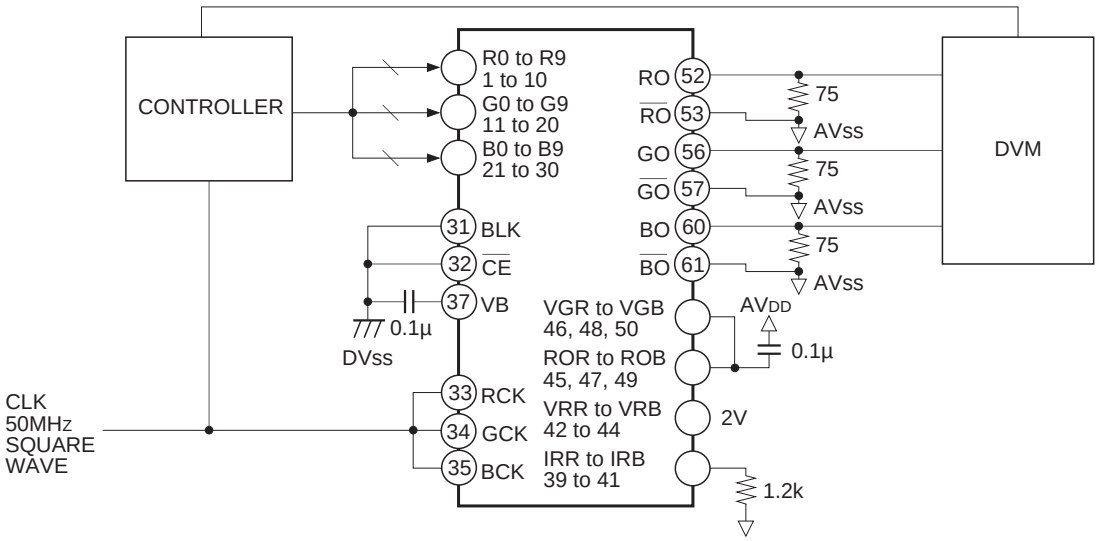
Test Circuit



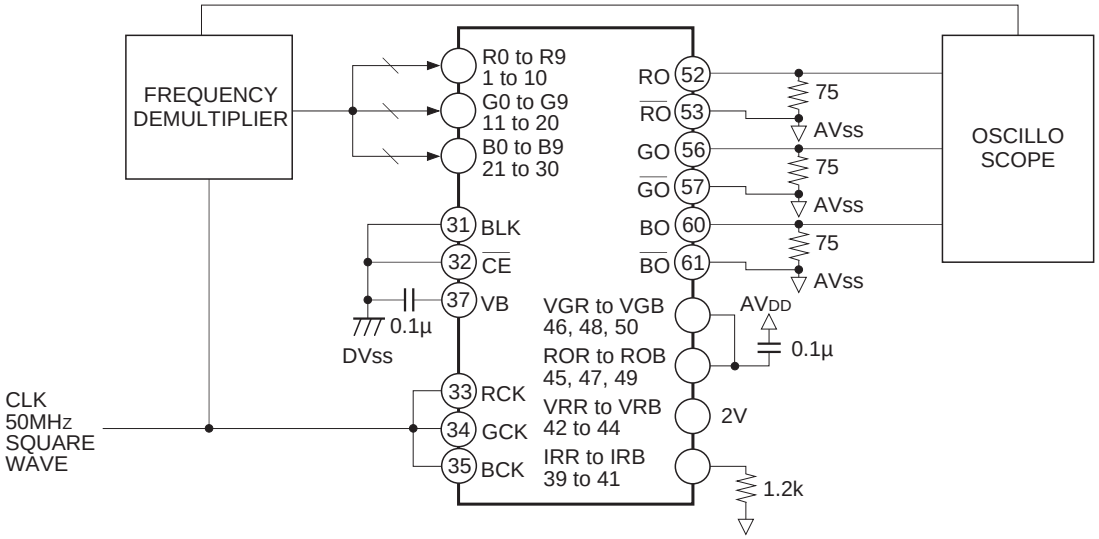
Cross Talk Test Circuit



DC Characteristics Test Circuit

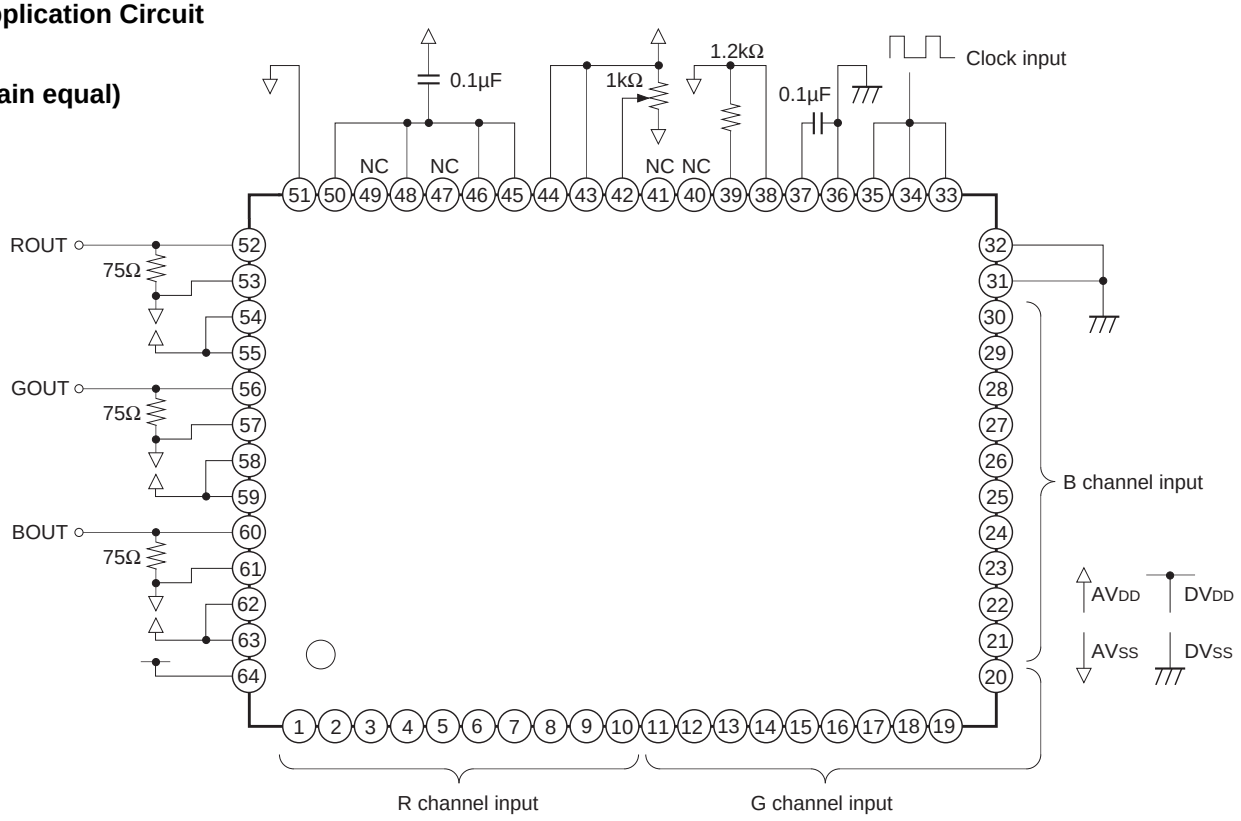


Propagation Delay Time Test Circuit

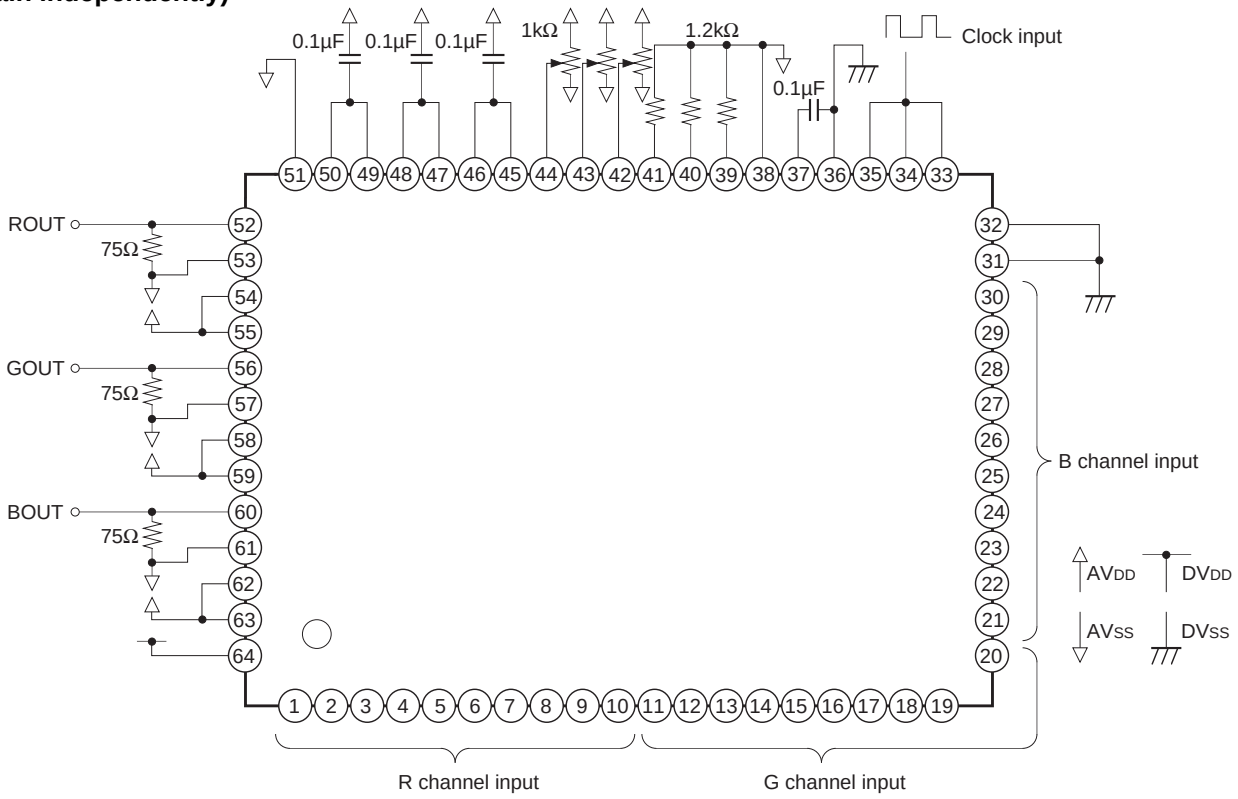


Application Circuit

(Gain equal)



(Gain independently)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

- How to select the output resistance

  The CXD2308Q is a D/A converter of the current output type. To obtain the output voltage connect the resistance to RO, GO and BO pin. For specifications we have:

  Output full scale voltage V_{FS}=1.8 to 2.0 [V]

  Output full scale current I_{FS}=less than 30 [mA]

  Calculate the output resistance value from the relation of $V_{FS}=I_{FS} \times R_{OUT}$. Also, 16 times resistance of the output resistance is connected to reference current pin IRR, IRG and IRB. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute.

  Here please note that V_{FS} becomes $V_{FS}=V_{REF} \times 16R_{OUT}/R_{IR}$. V_{REF} is the voltage set at the VRR, VRG and VRB pins and R_{OUT} is the resistance connected to RO, GO and BO while R_{IR} is connected to IRR, IRG and IRB. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

  To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the setup time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.

- Power supply and ground

  To reduce noise effects separate analog and digital systems in the device periphery. For power supply pins, both digital and analog, bypass respective grounds by using a ceramic capacitor of about 0.1 µF, as close as possible to the pin.

- Latch up

  Analog and digital power supply have to be common at the PCB power supply source. This is to prevent latch up due to voltage difference between AV_{DD} and DV_{DD} pins when power supply is turned ON.

- $\overline{RO}$, $\overline{GO}$ and $\overline{BO}$ pins

  The $\overline{RO}$, $\overline{GO}$ and $\overline{BO}$ pins are the inverted current output pins described in the Pin Description. The sums shown below become the constant value for any input data.

  a) The sum of the currents output from RO and $\overline{RO}$
  b) The sum of the currents output from GO and $\overline{GO}$
  c) The sum of the currents output from BO and $\overline{BO}$

  However, the performances such as the linearity error of the inverted current output pin output current is not guaranteed.

- Output full-scale voltage

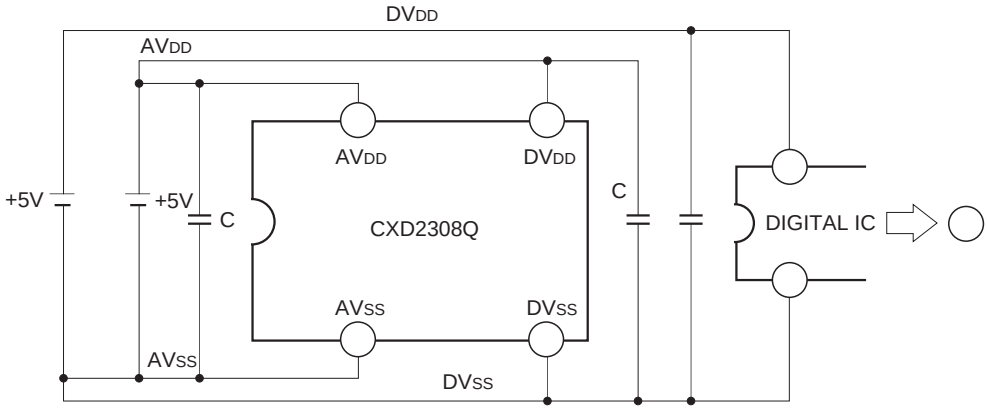
  For the applications using the RGB signal, the color balance may be broken up when the no-adjusted output full-scale voltage of RO, GO and BO are used.

Latch Up Prevention

The CXD2308Q is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} and DV_{DD}, when power supply is ON.

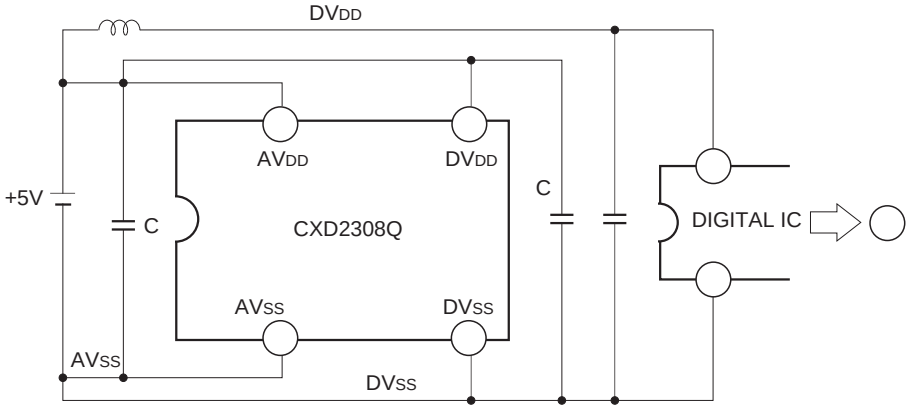
1. Correct usage

a. When analog and digital supplies are from different sources

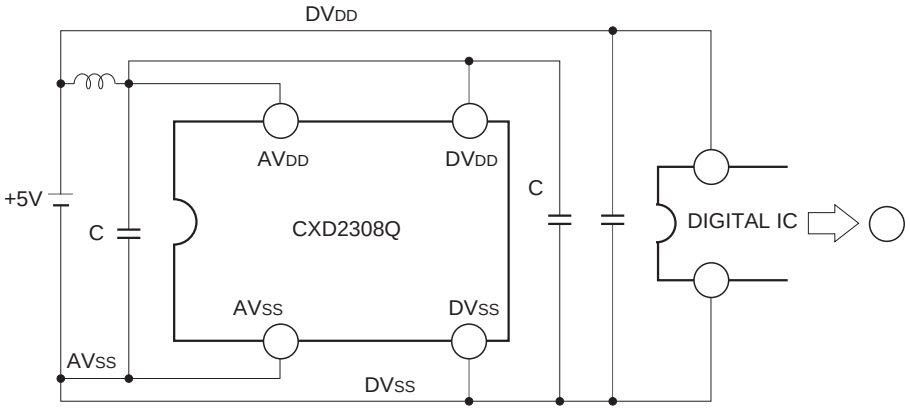


b. When analog and digital supplies are from a common source

(i)

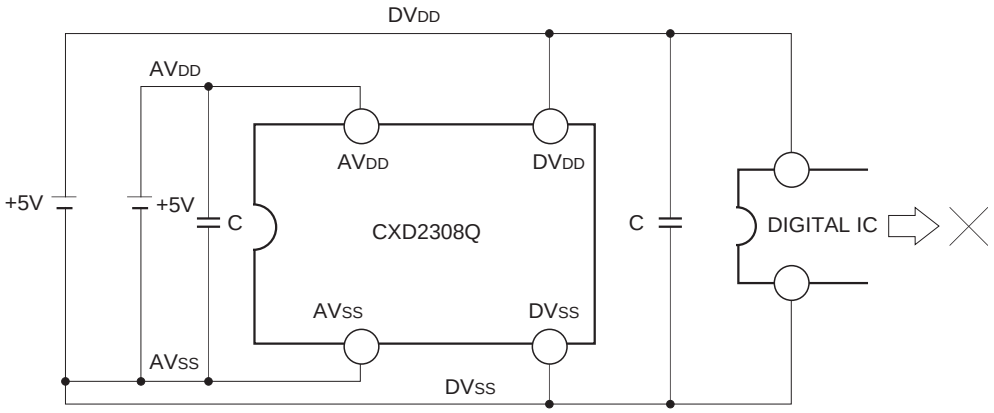


(ii)



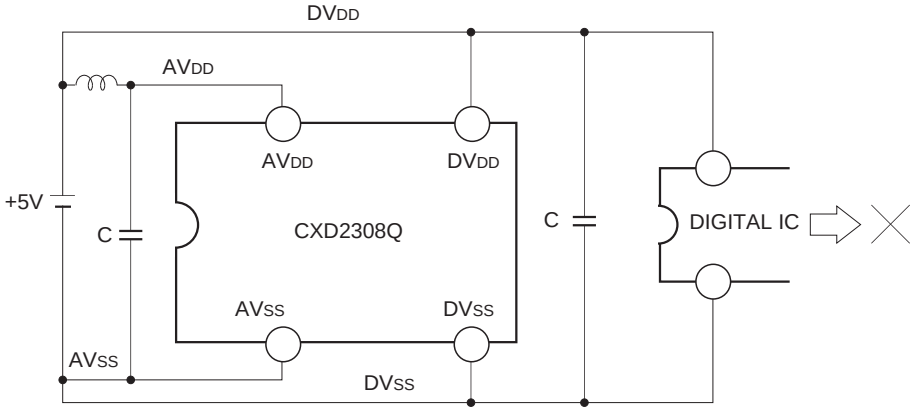
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

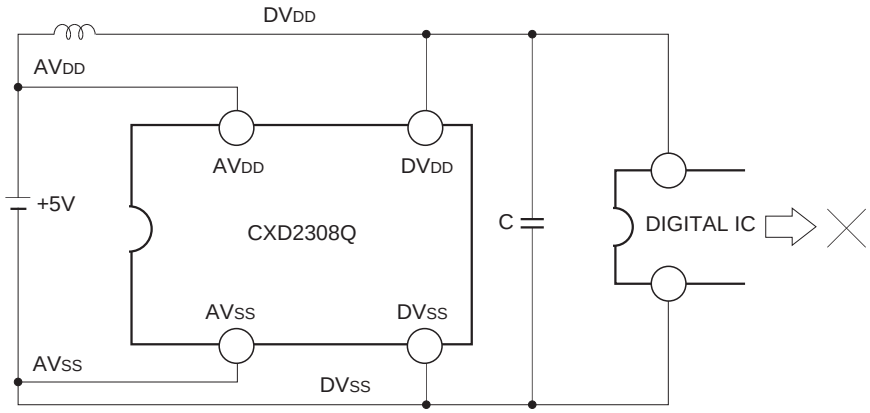


b. When analog and digital supplies are from common source

(i)

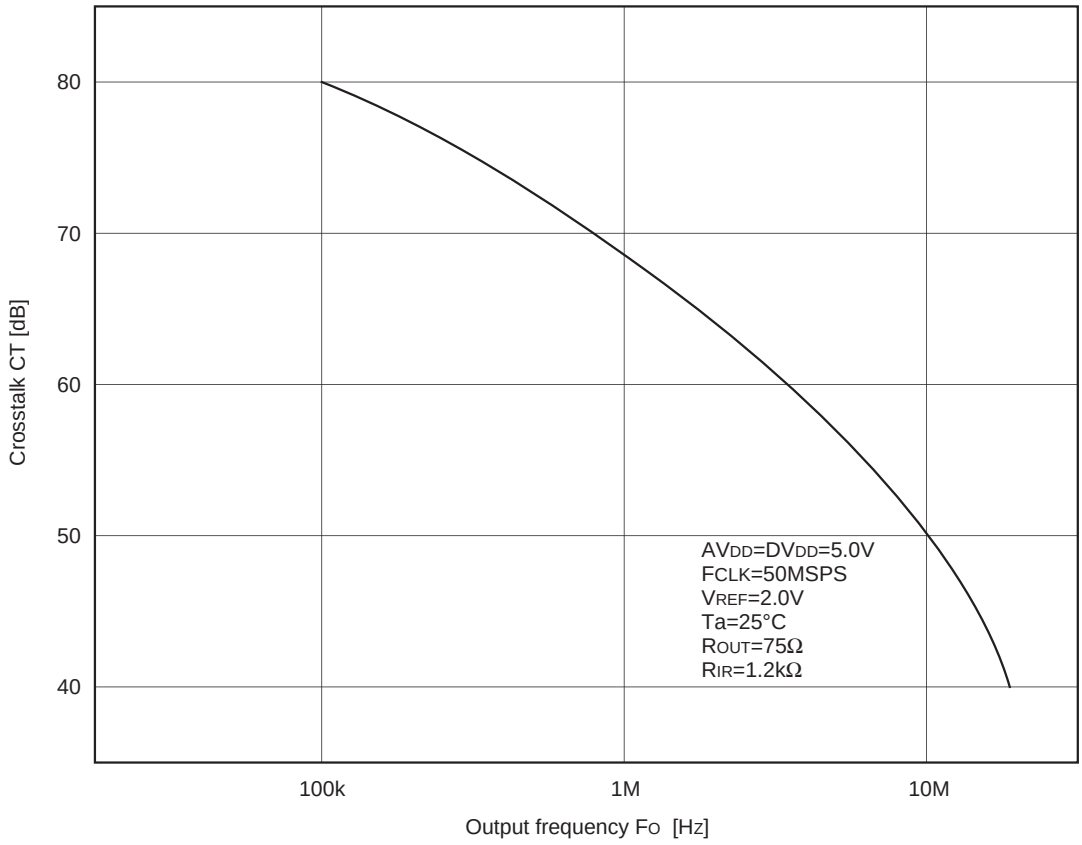


(ii)

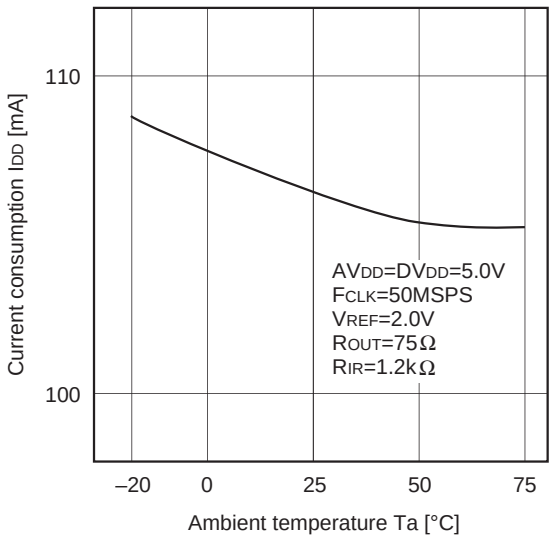


Example of Representative Characteristics

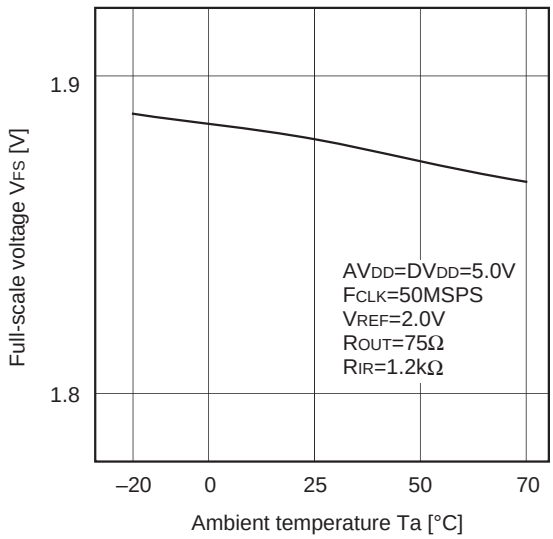
Output frequency vs. Crosstalk



Ambient temperature vs. Current consumption

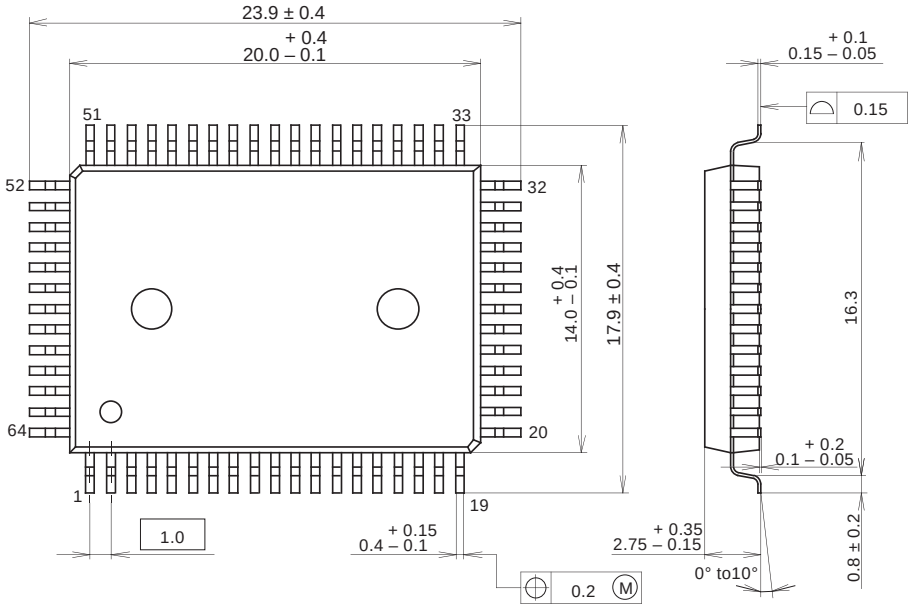


Ambient temperature vs. Full-scale voltage



Package Outline Unit : mm

64PIN QFP(PLASTIC)



SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g